What is claimed is:

1. A clock skew tolerant clocking scheme comprising:

a data stream;

a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse rising edge and a clock pulse falling edge and a clock pulse width between said clock pulse rising edge and said clock pulse falling edge;

a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, said second pulse signal being derived from said clock signal such that each of said second

pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

a first transparent pulse latch, said first pulse signal being operatively coupled to said first transparent pulse latch;

a second transparent pulse latch, said second pulse signal being operatively coupled to said second transparent pulse latch; wherein,

for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a rising edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a falling edge of said clock pulse; further wherein,

there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

2. The clock skew tolerant clocking scheme of Claim 1; wherein,

said first pulse width is ten to twenty-five percent of said clock cycle.

3. The clock skew tolerant clocking scheme of Claim 1; wherein,

said first pulse width is twenty percent of said clock cycle.

4. The clock skew tolerant clocking scheme of Claim 1; wherein,

said second pulse width is ten to twenty-five percent of said clock cycle.

5. The clock skew tolerant clocking scheme of Claim 1; wherein,

said second pulse width is twenty percent of said clock cycle.

6. The clock skew tolerant clocking scheme of Claim 1; wherein,

said first pulse width is equal to said second pulse width.

7. The clock skew tolerant clocking scheme of Claim 6; wherein,

said first pulse width and said second pulse width are ten to twenty-five percent of said clock cycle.

8. The clock skew tolerant clocking scheme of Claim 6; wherein,

said first pulse width and said second pulse width are twenty percent of said clock cycle.

9. The clock skew tolerant clocking scheme of Claim 1; wherein,

said first pulse signal and said second pulse signal are generated by pulse generators.

10. The clock skew tolerant clocking scheme of Claim 1; wherein,

said first pulse signal is generated by a first local pulse generator operatively coupled to said first transparent pulse latch; and

said second pulse signal is generated by a second local pulse generator operatively coupled to said second transparent pulse latch.

11. A method for clocking combinational logic blocks said method comprising:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse rising edge and a clock pulse falling edge and a clock pulse width between said clock pulse rising edge and said clock pulse falling edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, said second pulse signal being derived from said clock signal such that each of said

second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a rising edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a falling edge of said clock pulse; wherein,

there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

12. The method for clocking combinational logic blocks of Claim 11; wherein,

said first pulse width is ten to twenty-five percent of said clock cycle.

13. The method for clocking combinational logic blocks of Claim 11; wherein,

said first pulse width is twenty percent of said clock cycle.

14. The method for clocking combinational logic blocks of Claim 11; wherein,

said second pulse width is ten to twenty-five percent of said clock cycle.

15. The method for clocking combinational logic blocks of Claim 11; wherein,

said second pulse width is twenty percent of said clock cycle.

16. The method for clocking combinational logic blocks of Claim 11; wherein,

said first pulse width is equal to said second pulse width.

17. The method for clocking combinational logic blocks of Claim 16; wherein,

said first pulse width and said second pulse width are ten to twenty-five percent of said clock cycle.

18. The method for clocking combinational logic blocks of Claim 16; wherein,

said first pulse width and said second pulse width are twenty percent of said clock cycle.

19. The method for clocking combinational logic blocks of Claim 11; wherein,

said first pulse signal and said second pulse signal are generated by pulse generators.

20. The method for clocking combinational logic blocks of Claim 11; wherein,

said first pulse signal is generated by a first local pulse generator operatively coupled to said first transparent pulse latch; and

said second pulse signal is generated by a second local pulse generator operatively coupled to said second transparent pulse latch.

21. A method for creating a clock skew tolerate computer pipeline comprising;

providing a plurality of pipeline stages, each of said stages comprising combinational logic blocks, for each of said combinational logic blocks:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse rising edge and a clock pulse falling edge and a clock pulse width between said clock pulse rising edge and said clock pulse falling edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses

corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a rising edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a falling edge of said clock pulse; wherein,

there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

22. The method of Claim 21; wherein,

said first pulse width is ten to twenty-five percent of said clock cycle.

23. The method of Claim 21; wherein,

said first pulse width is twenty percent of said clock cycle.

24. The method of Claim 21; wherein,

said second pulse width is ten to twenty-five percent of said clock cycle.

25. The method of Claim 21; wherein,

said second pulse width is twenty percent of said clock cycle.

26. The method of Claim 21; wherein,
said first pulse width is equal to said second pulse width.

27. The method of Claim 26; wherein,
said first pulse width and said second pulse width are ten to twenty-five percent of said clock cycle.

28. The method of Claim 26; wherein,
said first pulse width and said second pulse width are twenty percent of said clock cycle.

29. The method of Claim 21; wherein,
said first pulse signal and said second pulse signal are generated by pulse generators.

30. The method of Claim 21; wherein,
said first pulse signal is generated by a first local pulse generator operatively coupled to said first transparent pulse latch; and
said second pulse signal is generated by a second local pulse generator operatively coupled to said second transparent pulse latch.

31. A clock skew tolerant clocking scheme comprising:
a data stream;
a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse falling edge and a clock pulse rising edge and a clock pulse width between said clock pulse falling edge and said clock pulse rising edge;

a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

a first transparent pulse latch, said first pulse signal being operatively coupled to said first transparent pulse latch;

a second transparent pulse latch, said second pulse signal being operatively coupled to said second transparent pulse latch; wherein,

for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a falling edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a rising edge of said clock pulse; further wherein,

there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

32. A method for clocking combinational logic blocks said method comprising:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse falling edge and a clock pulse rising edge and a clock pulse width between said clock pulse falling edge and said clock pulse rising edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a falling edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a rising edge of said clock pulse; wherein,

there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

33. A method for creating a clock skew tolerate computer pipeline comprising;

providing a plurality of pipeline stages, each of said stages comprising combinational logic blocks, for each of said combinational logic blocks:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse falling edge and a clock pulse rising edge and a clock pulse width between said clock pulse falling edge and said clock pulse rising edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse

rising edges of said second pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a falling edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a rising edge of said clock pulse; wherein,

there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

34. A clock skew tolerant clocking scheme comprising:

a data stream;

a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse first edge and a clock pulse second edge and a clock pulse width between said clock pulse first edge and said clock pulse second edge;

a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse first edge and a first pulse second edge and a first pulse width between said first

pulse first edge and said first pulse second edge, said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse first edges of said first pulses are generated by a corresponding clock pulse first edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse first edge and a second pulse second edge and a second pulse width between said second pulse first edge and said second pulse second edge, said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse first edges of said second pulses are generated by a corresponding clock pulse second edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

a first transparent pulse latch, said first pulse signal being operatively coupled to said first transparent pulse latch;

a second transparent pulse latch, said second pulse signal being operatively coupled to said second transparent pulse latch; wherein,

for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a first edge of said clock pulse and a corresponding second pulse of said plurality of

second pulses of said second pulse signal generated by a second edge of said clock pulse; further wherein,

there is a frequency dependent separation window between a second edge of said first pulse and first edge of said corresponding second pulse such that race conditions are avoided.

35. A method for clocking combinational logic blocks said method comprising:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse first edge and a clock pulse second edge and a clock pulse width between said clock pulse first edge and said clock pulse second edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse first edge and a first pulse second edge and a first pulse width between said first pulse first edge and said first pulse second edge, said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse first edges of said first pulses are generated by a corresponding clock pulse first edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse first edge and a second pulse second edge and a second pulse width

between said second pulse first edge and said second pulse second edge, said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse first edges of said second pulses are generated by a corresponding clock pulse second edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a first edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a second edge of said clock pulse; wherein,

there is a frequency dependent separation window between a second edge of said first pulse and first edge of said corresponding second such that race conditions are avoided.

36. A method for creating a clock skew tolerate computer pipeline comprising;

providing a plurality of pipeline stages, each of said stages comprising combinational logic blocks, for each of said combinational logic blocks:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of

said plurality of clock pulses comprising a clock pulse first edge and a clock pulse second edge and a clock pulse width between said clock pulse first edge and said clock pulse second edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse first edge and a first pulse second edge and a first pulse width between said first pulse first edge and said first pulse second edge, said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse first edges of said first pulses are generated by a corresponding clock pulse first edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse first edge and a second pulse second edge and a second pulse width between said second pulse first edge and said second pulse second edge, said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse first edges of said second pulses are generated by a corresponding clock pulse second edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a first edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a second edge of said clock pulse;

wherein,

there is a frequency dependent separation window between a second edge of said first pulse and first edge of said corresponding second such that race conditions are avoided.